Listing of the Claims:

This listing of claims lists all of the claims currently pending in the present application.

1. (Cancelled)

2. (Previously presented) The memory subsystem of claim 4 wherein the first memory array comprises an embedded memory array.

3. (Original) The memory subsystem of claim 2 wherein the first memory controller includes a register to store a pointer value for each of the functional memory sub-arrays indicative of the block of memory to which a respective functional memory sub-array is assigned.

4. (Previously presented) A memory subsystem, comprising:

a first memory array segmented into a plurality of memory sub-arrays having at least one functional memory sub-array, each of the functional memory sub-arrays being assigned to a respective block of memory and any faulty memory sub-arrays being left unassigned;

a first memory controller coupled to receive memory access requests to a block of memory to which a functional memory sub-array from the first memory array is assigned and further coupled to the first memory array to access the functional memory sub-array assigned to the requested block of memory;

a second memory array segmented into a plurality of memory sub-arrays, a number of which are functional, each of the functional memory sub-arrays of the second memory array assigned to a respective block of memory and any faulty memory sub-arrays left unassigned;

a second memory controller coupled to receive memory access requests to a block of memory to which a functional memory sub-array of the second memory array is assigned and further coupled to the second memory array to access the functional memory sub-array assigned to the requested block of memory; and

a memory controller bus coupled between the first and second memory controllers to pass a memory access request from one memory controller to the other in response to receiving a memory access request to access a memory location within the memory array coupled to the other memory controller.

5. (Previously presented) The memory subsystem of claim 4 wherein the first and second memory controllers store a value indicative of the number of functional sub-arrays in the first memory array a second memory array, respectively.

6. (Previously presented) The memory subsystem of claim 4 wherein the first and second memory controllers further store a start and size value for the first and second memory array, respectively, the start and size values defining the addressable memory area of the respective memory array.

7. (Original) The memory subsystem of claim 6 wherein the start value stored by the second memory controller is the sum of the start value and the size value stored by the first memory controller.

8. (Cancelled)

9. (Previously presented) The memory subsystem of claim 10 wherein the first memory array comprises an embedded memory.

10. (Previously presented) A memory subsystem receiving memory access requests, comprising:

a first memory array segmented into a plurality of memory sub-arrays having at least one functional memory sub-array;

a first register to store pointer values directing access to each functional sub-array;

a first memory controller coupled to the first memory array and the first register to consult the pointer values and determine which functional memory sub-arrays to access in response to receiving the memory access requests;

a second memory array segmented into a plurality of memory sub-arrays, a number of which are functional;

a second register to store second pointer values directing access to each functional sub-array of the second memory array;

a second memory controller coupled to the second memory array and the second register to consult the pointer values and determine which of the memory sub-arrays of the second memory array to access in response to receiving the memory access requests; and

a memory controller bus coupled between the first and second memory controllers to pass the memory access request to the other memory controller when the memory access request is to a memory location in the other memory array.

11. (Original) The memory subsystem of claim 10 wherein the first and second registers further store a value indicative of the number of functional sub-arrays in the first memory array a second memory array, respectively.

12. (Original) The memory subsystem of claim 10 wherein the first and second registers further store a start and size value for the first and second memory array, respectively, the start and size values defining the addressable memory area of the respective memory arrays.

13. (Original) The memory subsystem of claim 12 wherein the start value stored by the second register is the sum of the start value and the size value stored by the first register.

14. (Cancelled)

15. (Previously presented) The memory subsystem of claim 16 wherein the memory array comprises an embedded memory array fabricated on a semiconductor substrate with the memory controller.

16. (Previously presented) A memory subsystem, comprising:

a memory array segmented into a plurality of memory sub-arrays;

a memory controller coupled to access the memory array and having a register including a plurality of data fields, the data fields storing a pointer value indicative of which memory sub-arrays are functional and which memory sub-arrays to access in response to the memory controller receiving a memory access request;

a second memory array segmented into a plurality of memory sub-arrays;

a second memory controller coupled to access the second memory array and having a register including a plurality of data fields, the data fields of the second memory controller storing a pointer value indicative of which memory sub-arrays of the second memory array are functional and which to access in response to the second memory controller receiving a memory access request; and

a memory controller bus coupled between the memory controller and the second memory controller on which the memory access request may be passed from one memory controller to the other.

17. (Original) The memory subsystem of claim 16 wherein the second memory array is an embedded memory fabricated on the same semiconductor substrate as the memory array.

18. (Previously presented) The memory subsystem of claim 16 wherein the register of the memory controller further includes a memory valid field storing a value indicative of the number of functional memory sub-arrays of the plurality of memory sub-arrays.

19. (Cancelled)

20. (Previously presented) The graphics processing system of claim 22 wherein the first memory array comprises an embedded memory array.

21. (Original) The graphics processing system of claim 20 wherein the first memory controller of the memory subsystem includes a register to store a pointer value for each of the functional memory sub-arrays indicative of the block of memory to which a respective functional memory sub-array is assigned.

22. (Previously presented) A graphics processing system, comprising:

a bus interface for coupling to a system bus;

a graphics processor coupled to the bus interface to process graphics data;

address and data busses coupled to the graphics processor to transfer address and graphics data to an from the graphics processor;

display logic coupled to the data bus to drive a display;

a memory request bus coupled to the graphics processor to transfer memory and access requests; and

a memory subsystem coupled to the memory request bus to receive and service memory access requests, the memory subsystem comprising:

a first memory array segmented into a plurality of memory sub-arrays, a number of which are functional, each of the functional memory sub-arrays being assigned to a respective block of memory and any faulty memory sub-arrays being left unassigned;

a first memory controller coupled to receive memory access requests to a block of memory to which a functional memory sub-array from the first memory array is assigned and further coupled to the first memory array to access the functional memory sub-array assigned to the requested block of memory;

a second memory array segmented into a plurality of memory sub-arrays, a number of which are functional, each of the functional memory sub-arrays of the second

memory array assigned to a respective block of memory and any faulty memory sub-arrays left unassigned;

a second memory controller coupled to receive memory access requests to a block of memory to which a functional memory sub-array of the second memory array is assigned and further coupled to the second memory array to access the functional memory sub-array assigned to the requested block of memory; and

a memory controller bus coupled between the first and second memory controllers to pass a memory access request from one memory controller to the other in response to receiving a memory access request to access a memory location within the memory array coupled to the other memory controller.

23. (Previously presented) The graphics processing system of claim 22 wherein the first and second memory controllers of the memory subsystem store a value indicative of the number of functional sub-arrays in the first memory array a second memory array, respectively.

24. (Previously presented) The graphics processing system of claim 22 wherein the first and second memory controllers of the memory subsystem further store a start and size value for the first and second memory array, respectively, the start and size values defining the addressable memory area of the respective memory array.

25. (Original) The graphics processing system of claim 24 wherein the start value stored by the second memory controller of the memory subsystem is the sum of the start value and the size value stored by the first memory controller.

26. (Cancelled)

27. (Previously presented) The computer system of claim 28 wherein the memory array of the graphics processing system comprises an embedded memory array fabricated on a semiconductor substrate with the memory controller.

28. (Previously presented) A computer system, comprising:

a system processor;

a system bus coupled to the system processor;

a system memory coupled to the system bus; and

a graphics processing system coupled to the system bus, the graphics processing system comprising:

a bus interface for coupling to a system bus;

a graphics processor coupled to the bus interface to process graphics data;

address and data busses coupled to the graphics processor to transfer address and graphics data to an from the graphics processor;

display logic coupled to the data bus to drive a display;

a memory request bus coupled to the graphics processor to transfer memory and access requests; and

a memory subsystem coupled to the memory request bus to receive and service memory access requests, the memory subsystem comprising:

a first memory array segmented into a plurality of memory sub-arrays;

a first memory controller coupled to the memory request bus to receive memory access requests and further coupled to access the memory array, the memory controller having a register including a plurality of data fields, the data fields storing a pointer value indicative of which memory sub-arrays are functional and which memory sub-arrays to access in response to the memory controller receiving memory access requests;

a second memory array segmented into a plurality of memory sub-arrays;

a second memory controller coupled to access the second memory array and having a register including a plurality of data fields, the data fields of the second memory controller storing a pointer value indicative of which memory sub-arrays of the second memory array are functional and which to access in response to the second memory controller receiving a memory access request; and

a memory controller bus coupled between the memory controller and the second memory controller on which the memory access request may be passed from one memory controller to the other.

29. (Original) The computer system of claim 28 wherein the second memory array of the memory subsystem comprises an embedded memory fabricated on the same semiconductor substrate as the memory array.

30. (Previously presented) The computer system of claim 28 wherein the register of the memory controller further includes a memory valid field storing a value indicative of the number of functional memory sub-arrays of the plurality of memory sub-arrays.

31. (Cancelled)

32. (Previously presented) The method of claim 35 wherein assigning each functional memory sub-array comprises storing for each memory block a pointer value identifying the respective functional memory sub-array to which it is assigned.

33. (Original) The method of claim 32, further comprising storing a valid value indicative of the number of functional memory sub-arrays.

34. (Previously presented) The method of claim 35 wherein the memory array comprises an embedded memory array.

35. (Previously presented) A method of accessing a memory array segmented into a plurality of memory sub-arrays, at least one of the memory sub-arrays being functional, the method comprising:

assigning each functional memory sub-array of the memory array to a respective memory block and leaving any faulty memory sub-arrays unassigned;

in response to receiving a memory access request to access a particular memory block, accessing the memory sub-array assigned to the particular memory block;

storing start address and size values defining an addressable memory area of the memory array;

determining from the start address and size values whether the particular memory block of the memory access request is assigned to a memory sub-array within the addressable memory area of the memory array; and

servicing the memory access request if the particular memory block is determined to be assigned to a memory sub-array within the addressable memory area of the memory array, otherwise passing the memory access request to another memory controller for servicing.

36. (Original) The method of claim 35, further comprising storing second start address and size values defining an addressable memory area of a second memory array, the second start address value equal to the sum of the start address and size values of the addressable memory area of the memory array.

37. (Original) A method of accessing an embedded memory array segmented into a plurality of memory sub-arrays, at least one of the memory sub-arrays being functional, the method comprising:

storing for each of a plurality of memory blocks a pointer value identifying a functional memory sub-array assigned thereto;

storing start address and size values defining an addressable memory area of the embedded memory array;

in response to receiving a memory access request to access a particular memory block, determining from the start address and size values whether the particular memory block is assigned to a memory sub-array within the addressable memory area of the embedded memory array; and

accessing the memory sub-array identified by the pointer value stored for the particular memory block if the particular memory block is determined to be assigned to a

memory sub-array within the addressable memory area of the embedded memory array, otherwise passing the memory access request to another memory controller for servicing.

38. (Original) The method of claim 37, further comprising storing second start address and size values defining an addressable memory area of a second embedded memory array, the second start address value equal to the sum of the start address and size values of the addressable memory area of the embedded memory array.

39. (Original) The method of claim 37, further comprising storing a valid value indicative of the number of function memory sub-arrays of the memory array.